Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 3. (Canceled)

4. (Previously Presented) A semiconductor integrated circuit for processing a plurality of received broadcast signals, the broadcast signals being of a type each having a different respective digital code, the semiconductor integrated circuit comprising:

a digital sampler;

a sample reducer; and

a plurality of correlators being arranged to be operable in two modes wherein:

in an acquisition mode:

the digital sampler is adapted to sample the received broadcast signals to produce a digital bit stream at a first bit rate;

the sample reducer is adapted to reduce bits of the digital bit stream by combining groups of N bits together to produce a reduced digital bit stream;

the plurality of correlators is adapted to receive the reduced digital bit stream at a second bit rate, being higher than the first bit rate, and each of the plurality of correlators is adapted to correlate the reduced digital bit stream with a same locally generated version of one of the different digital codes; and

in a track mode:

the digital sampler is adapted to sample the received broadcast signals to produce a digital bit stream at the first bit rate and to provide the digital bit stream direct to each of the plurality of correlators, each correlator is adapted to correlate the digital bit stream with a different locally generated version of one of the digital codes,

wherein for the acquisition mode, the sample reducer includes an adder to add the groups of N bits,

wherein in the acquisition mode, the adder is adapted to provide a digital output representative of a value of a sum of the N bits, and

wherein in the acquisition mode, the adder is adapted to provide an output having a first logic state if the sum of the N bits is greater than a given value and an output having a second logic state opposite to said first logic state if the sum of N bits is less than the given value.

5. (Currently Amended) The semiconductor integrated circuit according to claim 4 wherein in acquisition mode, the adder is adapted to alternately provide said first logic state and said second logic state if the sum of the N bits is equal to the given value.

6. (Previously Presented) The semiconductor integrated circuit according to claim 4 wherein in acquisition mode the second bit rate is a factor M higher than the first bit rate.

7. (Previously Presented) The semiconductor integrated circuit according to claim 6 wherein there are Y correlators such that in acquisition mode a correlation rate is a factor X = N (bits) x M (bit rate factor) x Y(correlators) faster than a correlation rate in the track mode for one of the digital codes.

8. (Previously Presented) The semiconductor integrated circuit according to claim 7 wherein the factor X is chosen to be substantially equal or greater than twice a number of bits in the code, wherein all possible correlations of the code are performed before the code repeats.

9. (Previously Presented) The semiconductor integrated circuit according to claim 8 wherein the digital code is a GPS position code of 1,023 bits and wherein the factor X is arranged to be 2,048.

10. (Previously Presented) The semiconductor integrated circuit according to claim 4, further comprising a memory to receive the reduced digital bit stream and to output the reduced digital bit stream at the second bit rate to the plurality of correlators.

11. (Previously Presented) The semiconductor integrated circuit according to claim 10 wherein the memory includes a circulating shift register.

12. (Previously Presented) The semiconductor integrated circuit according to claim 11 wherein the circulating shift register receives the reduced digital bit stream at a rate equal to the first bit rate divided by N and circulates at the second bit rate.

13. (Previously Presented) The semiconductor integrated circuit according to claim 10 wherein the memory includes two shift registers arranged to alternately receive the reduced digital bit stream while another of the two shift registers circulates at the second bit rate.

14. – 16. (Canceled)

17. (Previously Presented) A method of processing a plurality of received broadcast signals each having a different respective digital code, the method comprising:

sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

reducing bits of the digital bit stream by combining groups of N bits to produce a reduced bit stream;

correlating the reduced digital bit stream at a second bit rate using a plurality of correlators each correlating the reduced digital bit stream with a same one of a locally generated version of the digital codes to acquire the broadcast signals; and

subsequently correlating the digital bit stream at the first bit rate using the plurality of correlators each correlating the digital bit stream with a locally generated version of a different one of the digital codes to track the previously acquired signals,

wherein the reducing the bits of the digital bit stream includes summing groups of N bits,

wherein the summing produces a digital output representative of the sum, and

wherein the summing produces a first logic state if the sum of N bits is greater than a given value and a second logic state opposite to said first logic state if the sum is less than the given value.

18. (Previously Presented) The method according to claim 17 wherein the summing alternately provides said first logic state and second logic state if the sum of N bits is equal to the given value.

19. (Previously Presented) The method according to claim 17 wherein the second bit rate is a factor M higher than the first bit rate.

20. (Previously Presented) The method according to claim 19 wherein there are Y correlators such that when correlating to acquire, a correlation rate is a factor X = N (bits) x M (bit rate factor) x Y (correlators) faster than a correlation rate when tracking the acquired signals.

21. (Previously Presented) The method according to claim 20 wherein the factor X is chosen to be substantially equal or greater than twice a number of bits in the code, wherein all possible correlations of the code are performed before the code repeats.

22. (Canceled)

23. (Previously Presented) The apparatus of claim 25 wherein the correlator unit includes a plurality of correlators to correlate the reduced digital bit stream at the second bit rate with a same one of the digital codes in the acquisition mode.

24. (Previously Presented) The apparatus of claim 25 wherein the digital codes for the correlations include locally generated versions of the digital codes of the received broadcast signals.

25. (Previously Presented) An apparatus to process a plurality of received broadcast signals having digital codes, the apparatus comprising:

a sampler unit to sample the received broadcast signals to produce a digital bit stream at a first bit rate in an acquisition mode;

a reducer unit coupled to the sampler unit to reduce a number of bits of the digital bit stream via combination of groups of N bits together to produce a reduced digital bit stream in the acquisition mode; and

a correlator unit coupled to the reducer unit to receive the reduced digital bit stream at a second bit rate and to correlate the reduced digital bit stream with one of the digital codes in the acquisition mode, and wherein the sampler unit is coupled to the correlator unit to directly provide the digital bit stream at the first bit rate to the correlator unit in a track mode and further wherein the correlator unit is adapted to correlate that digital bit stream with a different one of the digital codes in the track mode,

wherein the reducer unit includes an adder to add the groups of N bits in the acquisition mode to obtain a sum, and wherein further in the acquisition mode:

the adder is coupled to provide a digital output representative of the sum;

the adder is coupled to provide a first binary value if the sum is greater than a given value and a second binary value if the sum is less than the given value; and

the adder is coupled to alternately provide the first binary value and the second binary value if the sum is equal to the given value.

26. (Previously Presented) The apparatus of claim 25 wherein the second bit rate is higher than the first bit rate in the acquisition mode.

27. (Previously Presented) The apparatus of claim 25, further comprising a memory arrangement coupled to the correlator unit to receive the reduced digital bit stream and to output the reduced digital bit stream to the correlator unit at the second bit rate.

28. (Previously Presented) The apparatus of claim 27 wherein the memory arrangement includes a circulating shift register.

29. (Canceled)

30. (Previously Presented) The system of claim 31 wherein the means for reducing the number of bits of the digital bit stream produces the reduced digital bit stream at a second bit rate higher than the first bit rate.

31. (Previously Presented) A system to process a plurality of received broadcast signals having digital codes, the system comprising:

means for sampling the received broadcast signals to produce a digital bit stream at a first bit rate;

means for reducing a number of bits of the digital bit stream by combining groups of N bits to produce a reduced digital bit stream; and

means for correlating the reduced digital bit stream with one of the digital codes to acquire the broadcast signals, and for correlating the digital bit stream at the first bit rate with a different one of the digital codes to track the acquired broadcast signals,

wherein the means for reducing the number of bits of the digital bit stream by combining groups of N bits includes means for summing the groups of N bits to obtain a sum, the means for summing including:

means for providing a first binary value if the sum is greater than a given value and a second binary value if the sum is less than the given value; and

means for alternately providing the first binary value and the second binary value if the sum is equal to the given value.

32. (Previously Presented) The system of claim 31 wherein the broadcast signals include global position (GPS) signals.

33. (Previously Presented) The apparatus of claim 25 wherein the broadcast signals include global position (GPS) signals.

34. (Previously Presented) The method according to claim 17 wherein the broadcast signals include global position (GPS) signals.

35. (Previously Presented) The semiconductor integrated circuit according to claim 4 wherein the broadcast signals include global position (GPS) signals.